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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,329	12/03/2001	Jeff L. Hunter	TI-33316	5547

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EXAMINER

YIGDALL, MICHAEL J

ART UNIT	PAPER NUMBER
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2192

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/998,329

Applicant(s)

HUNTER ET AL.

Examiner

Michael J. Yigdall

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-7 and 13-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-6 and 13-15 is/are allowed.
- 6) ☒ Claim(s) 7, 16 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 6/9/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment and response filed on June 9, 2005 has been fully considered. Claims 1, 8-12, 18 and 19 have been canceled and claims 2, 6, 7, 13 and 16 have been amended. Claims 2-7 and 13-17 remain pending.

Response to Arguments

2. Applicant's arguments with respect to claims 2-6 and 13-17 (Applicant's remarks, pages 11-19) have been fully considered and are persuasive. The rejection of claims 2-6 and 13-17 under 35 U.S.C. 103(a) has been withdrawn.
3. Applicant's arguments with respect to claim 7 have been fully considered but they are not persuasive.

Applicant contends, "The memory map taught in Tarui et al fails to indicate whether the processor may read/write or read only some parts of memory" (Applicant's remarks, page 11, bottom). However, as set forth in the claim rejections below, Mahin teaches a memory map that expressly indicates whether memory segments are read-only or read/write (see, for example, column 2, lines 6-17).

Applicant contends that the cited portions of Falik fail to teach the recited limitations of "setting a first software breakpoint in a shared memory location" (Applicant's remarks, page 14, middle) and "clearing the first software breakpoint in the shared memory location" (Applicant's remarks, page 15, middle).

However, Falik teaches an ABORT mask register in the test access port (see, for example, column 5, lines 18-22), and DBGABORT and DBGISESRC registers in the interrupt controller (see, for example, column 7, lines 15-20). The test access port and the interrupt controller are included in the debugger interface module (see, for example, debugger I/F module 1841, TAP 102 and ISE interrupt control 104 in FIG. 1), which is shared among the processors (see, for example, FIG. 21). Accordingly, the bit locations in the registers are considered “shared memory locations.” Falik teaches that these registers control the breakpoints for all processors (see, for example, column 16, lines 1-5, 25-27 and 36-39). A breakpoint is “set” such that the debugger of each processor is notified as needed (see, for example, column 16, lines 40-50) and subsequently “cleared” in a similar manner (see, for example, column 17, lines 37-48). As Applicant notes, Falik does teach actions that are taken upon reaching and after reaching a breakpoint. Nonetheless, Falik further teaches that the breakpoint is “set” and “cleared” for the plurality of processors by writing to the registers noted above. The plain language of the claim does not exclude the teachings of Falik. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Oath/Declaration

4. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because although it acknowledges the duty to disclose in accordance with 37 CFR 1.56(a), it does not state that the person making the oath or

declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in 37 CFR 1.56, as required by 37 CFR 1.63(b)(3).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

With respect to claim 16 (currently amended), the claim recites, for example, “the first debug session” in line 10, “the shared memory location” in line 11, “the write request” in lines 13-14, and “the software memory map” in line 16. There is insufficient antecedent basis for these and other instances of these limitations in the claim.

With respect to claim 17, the claim is dependent upon claim 16.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,065,078 to Falik et al. (art of record, "Falik") in view of U.S. Pat. No. 6,088,770 to Tarui et al. (art of record, "Tarui") in view of U.S. Pat. No. 5,761,719 to Mahin et al. (art now made of record, "Mahin").

With respect to claim 7 (currently amended), Falik discloses a software development method for debugging software on a target system having a plurality of processors (see, for example, column 1, lines 34-39) configured with shared memory (see, for example, column 17, lines 46-48).

Although Falik discloses defining the processor configuration of the target system (see, for example, column 3, lines 9-16), Falik does not expressly disclose the steps of:

- (a) receiving user input to define a hardware configuration of the target system; and
- (b) creating a software memory map of how each of the plurality of processors may access memory including whether each of said plurality of processors may read from and write to a range of memory or may only read from said range of memory.

However, Tarui teaches defining hardware configuration information for the target system (see, for example, column 9, lines 12-31), as in step (a) above, and further teaches receiving the hardware configuration information to create a memory map of the local and shared memory, as in step (b) above. Like Falik, the target system in Tarui is a shared memory multiprocessor system (see, for example, column 6, lines 5-8). The memory map of Tarui is used, for example, to determine which processor controls the memory sought by an access request on the shared memory bus (see, for example, column 9, lines 1-11).

Although Tarui does not expressly disclose that the memory map includes whether each of said plurality of processors may read from and write to a range of memory or may only read from said range of memory, Mahin teaches a memory map that includes whether or not a memory segment or memory range is cacheable, and whether the memory range is read-only or read/write (see, for example, column 2, lines 6-17). The memory map eliminates the need for specialized hardware processing to determine whether a memory range is read-only or read/write (see, for example, column 2, lines 37-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the software development method of Falik with the shared memory features taught by Tarui. One of ordinary skill in the art would have been motivated to provide a memory map, such as taught by Tarui, so as to determine which of the plurality of processors disclosed by Falik controls which range of memory. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the memory map whether each of the processors may read from and write to or only read from the range of memory, such as taught by Mahin. One of ordinary skill in the art would have been motivated to provide such information taught by Mahin so as to eliminate the need for any additional specialized hardware processing in Falik to determine whether the processor has read/write or read-only access to the range of memory.

Falik also discloses the steps of:

(c) loading drivers for each of the plurality of processors (see, for example, FIG. 18, which shows a driver for each processor);

(d) activating a first debug session associated with a first processor of the plurality of processors (see, for example, column 2, lines 37-43, which shows a separate debugger or debug session for each processor);

(e) activating at least a second debug session associated with a second processor of the plurality of processors (see, for example, column 2, lines 37-43, which shows a separate debugger or debug session for each processor) wherein each debug session is operable to transmit read requests and write requests to its associated processor (see, for example, column 4, lines 30-37, which shows that each debugger can transmit messages or requests to its associated processor); and

(f) processing shared memory access requests via a software memory bus (see, for example, column 2, line 63 to column 3, line 3, which shows an interface or bus for processing shared resource and shared memory access requests), in which processing of shared memory access requests via the software memory bus uses a method for maintaining coherency of software breakpoints in shared memory when debugging a multiple processor system (see, for example, column 16, lines 36-54), the method comprising the steps of:

(i) setting a first software breakpoint in a shared memory location in the first debug session such that all debug sessions are notified of the setting of the breakpoint (see, for example, column 16, lines 40-50, which shows setting a breakpoint such that the monitor or debug session of each processor is notified); and

(ii) clearing the first software breakpoint in the shared memory location in the second debug session such that all debug sessions are notified of the clearing of the

breakpoint (see, for example, column 17, lines 37-48, which shows clearing the breakpoint such that the monitor or debug session of each processor is notified).

Allowable Subject Matter

9. Claims 2-6 and 13-15 are allowed. Claims 16 and 17 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not expressly teach a software development method for debugging software on a target system having a plurality of processors configured with shared memory comprising the exact steps and limitations recited in the claims. Specifically, the prior art of record does not teach activating a first debug session associated with a first processor and a second debug session associated with a second processor combined with the steps of (a) detecting a write request to a shared memory location by the first debug session, (b) selecting the first processor to perform the write request if the first processor associated with the first debug session has write access to the shared memory location, otherwise (c) searching a software memory map to determine if the second processor has write access to the shared memory location and selecting the second processor to perform the write request, and (d) passing the write request initiated by the first debug session to the selected processor for execution, as recited in independent claim 2. Similarly, the prior art of record does not teach activating a first debug session associated with a first processor and a second debug session associated with a second processor combined with the steps of (a) detecting a write request to a shared memory

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location by the first debug session, (b) passing the write request to the first processor for execution, (c) searching a software memory map for a plurality of processors that have read access to the shared memory location, (d) broadcasting the write request to the plurality of processors, and (e) performing cache coherency updates in response to the write request in each of the plurality of processors, as recited in independent claim 13.

11. As allowable subject matter has been indicated, Applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707.

The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

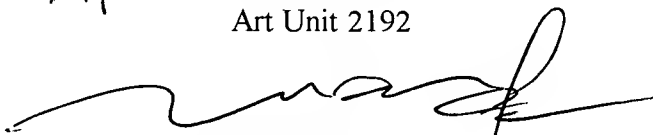
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2192

mjy



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SUPERVISORY PATENT EXAMINER